Claims

What is claimed:

1. A current threshold range detector comprising:
   a first test memory cell for sensing a first current threshold; and
   a second test memory cell for sensing a second current threshold.

2. The detector of claim 1, wherein a current applied to the first test memory cell and the second test memory cell comprises alternating polarity pulses.

3. The detector of claim 1, wherein the first test memory cell is a first MRAM cell that is configured to switch magnetic orientations when a magnetic field created by a current having a magnitude at least as great as the first current threshold is applied to the first MRAM cell.

4. The detector of claim 1, wherein the second test memory cell is a second MRAM cell that is configured to switch magnetic orientations when a magnetic field created by a current having a magnitude at least as great as the second current threshold is applied to the second MRAM cell.

5. The detector of claim 3, wherein a coercivity of the first MRAM cell is selected by pre-selection of at least one of a size of the first MRAM cell, a shape of the first MRAM cell, a shape of a proximate write conductor, a distance between the first MRAM cell and the write conductor.

6. The detector of claim 4, wherein a coercivity of the second MRAM cell is selected by pre-selection of at least one of a size of the second MRAM cell, a shape of the second MRAM cell, a shape of a proximate write conductor, a distance between the second MRAM cell and the write conductor.

7. A magnetic memory cell write current threshold detector comprising:

a first MRAM test cell receiving a write current and sensing when the write current exceeds a first threshold; and

a second MRAM test cell receiving the write current and sensing when the write current exceeds a second threshold.

8. The detector of claim 7, wherein the first threshold current corresponds with a magnitude of write current to reliably switch MRAM cells of an array of MRAM cells.

9. The detector of claim 7, wherein the second threshold current corresponds with a magnitude of write current to reliably switch MRAM cells of an array of MRAM cells without resulting in half select errors.

10. The detector of claim 7, wherein the write current comprises alternating polarity pulses.

11. The detector of claim 7, wherein a coercivity of the first MRAM test cell is pre-selected by pre-selecting a size and shape of the first MRAM test cell.

12. The detector of claim 7, wherein a coercivity of the second MRAM test cell is pre-selected by pre-selecting a size and shape of the second MRAM test cell.

13. The detector of claim 7, wherein the first MRAM test cell and the second MRAM test cell are substantially larger than the MRAM cells of the array of MRAM cells.

14. An array of magnetic memory cells comprising:

a write current generator for generating a write current for writing to selected memory cells within the array of magnetic memory cells;

a first test magnetic memory cell for sensing when a magnitude of the write current is large enough to reliably write to the magnetic memory cells;

a second test magnetic memory cell for sensing when the magnitude of the write current is so large that half select errors occur when writing to the magnetic memory cells.

15. The array of magnetic memory cells of claim 14, wherein the first test magnetic memory cell and the second test magnetic memory cell are substantially larger than the memory cells of the array of magnetic memory cells.

16. The array of magnetic memory cells of claim 14, wherein if the first test magnetic memory cell does not change magnetic orientations when sensing the write current, the write current is increased.

17. The array of magnetic memory cells of claim 14, wherein if the second test magnetic memory cell does change magnetic orientations when sensing the write current, the write current is decreased.

18. A method of selecting a magnetic memory cell write current comprising:

sensing the write current with a first test magnetic memory cell;

sensing the write current with a second test magnetic memory cell;

selecting the write current based upon the sensing of the first test magnetic memory cell and the second test magnetic memory cell.

19. The method of claim 18, wherein the first test magnetic memory cell changes magnetic orientation when the write current exceeds a first threshold.

20. The method of claim 18, wherein the second test magnetic memory cell changes magnetic orientation when the write current exceeds a second threshold.

21. The method of claim 18, wherein if the first test magnetic memory cell does not change magnetic orientations, then the write current is increased.

22. The method of claim 18, wherein if the second test magnetic memory cell changes magnetic orientations, then the write current is decreased.

23. A magnetic memory apparatus comprising:

an array of magnetic memory cells;

a write current generator for generating write current for writing to the magnetic memory cells;

means for sensing the write current with a first test magnetic memory cell;

means for sensing the write current with a second test magnetic memory cell;

means for selecting the write current based upon responses of the first test magnetic memory cell and the second test magnetic memory cell.

24. A computing system comprising:

a processor interfaced with an array of magnetic memory cells;

the array of magnetic memory cells comprising;

a write current generator for generating a write current for writing to selected memory cells within the array of magnetic memory cells;

a first test magnetic memory cell for sensing when a magnitude of the write current is large enough to reliably write to the magnetic memory cells;

a second test magnetic memory cell for sensing when the magnitude of the write current is so large that half select errors occur when writing to the magnetic memory cells.